1. (Currently Amended) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit connected thereto, said baseband processor comprising

a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit,

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to said radio circuit,

said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component for reducing an average DC signal component of the ~~decoded~~ information decoded by the modified Walsh code relative to that information being decoded by an unmodified Walsh code which, in combination with the AC-coupling to said at least one A/D converter enhances overall performance, and

a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

2. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

3. (Original) A spread spectrum radio transceiver according to claim 2 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third

format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

4. (Original) A spread spectrum radio transceiver according to claim 3 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

5. (Original) A spread spectrum radio transceiver according to claim 3 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

6. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

7. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

8. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

9. (Original) A spread spectrum radio transceiver according to claim 1 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

10. (Original) A spread spectrum radio transceiver according to claim 1 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel connected correlators connected to said modified Walsh function generator.

11. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

12. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

13. (Original) A spread spectrum radio transceiver according to claim 1 wherein said demodulator comprises clear channel assessing means for generating a clear channel assessment signal.

14. (Original) A spread spectrum radio transceiver according to claim 1 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator connected to said baseband processor; and

an up/down frequency converter connected to said quadrature intermediate frequency modulator/demodulator.

15. (Original) A spread spectrum radio transceiver according to claim 14 wherein said radio circuit further comprises:

a low noise amplifier having an output connected to an input of said up/down converter; and

a radio frequency power amplifier having an input connected to an output of said up/down converter.

16. (Original) A spread spectrum radio transceiver according to claim 15 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

17. (Currently Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~decoded~~ information decoded by the predetermined

orthogonal code relative to that information being decoded by the predetermined orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to the predetermined orthogonal code.

18. (Original) A baseband processor according to claim 17 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

19. (Original) A baseband processor according to claim 18 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

20. (Original) A baseband processor according to claim 19 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

21. (Original) A baseband processor according to claim 19 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

22. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

23. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

24. (Original) A baseband processor according to claim 17 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder.

25. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

26. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a bi-orthogonal code.

27. (Original) A baseband processor according to claim 17 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

28. (Original) A baseband processor according to claim 17 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

29. (Original) A baseband processor according to claim 17 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

30. (Original) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

means for operating in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate,

header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising

at least one correlator for decoding received information,

means for operating in one of the first and second formats,

header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,

a first carrier tracking loop for the third format, and

a second carrier tracking loop for the first and second formats.

31. (Original) A baseband processor according to claim 30 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

32. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

33. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

34. (Original) A baseband processor according to claim 30 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a

predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

35. (Original) A baseband processor according to claim 30 wherein said modulator comprises a scrambler; and

wherein said demodulator comprises a descrambler.

36. (Currently Amended) A modulator for a spread spectrum radio transceiver, said modulator comprising:

modulator means for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator means comprising at least one predetermined orthogonal code function encoder for encoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~encoded~~ information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state.

37. (Original) A modulator according to claim 36 wherein said modulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

38. (Original) A modulator according to claim 37 wherein said modulator means comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats.

39. (Original) A modulator according to claim 38 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

40. (Original) A modulator according to claim 36 wherein said modulator means further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder, and wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

41. (Original) A modulator according to claim 36 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

42. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

43. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a bi-orthogonal code.

44. (Currently Amended) A demodulator for a spread spectrum radio transceiver, said demodulator comprising:

demodulator means for spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator means comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have

a reduced DC signal component for reducing an average DC signal component of the ~~decoded~~ information decoded by the predetermined orthogonal code relative to that information being decoded by the predetermined orthogonal code in its unmodified state.

45. (Original) A demodulator according to claim 44 wherein said demodulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

46. (Original) A demodulator according to claim 45 wherein said demodulator means comprises header demodulator means for demodulating data packets including a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

47. (Original) A demodulator according to claim 46 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

48. (Original) A demodulator according to claim 46 wherein said demodulator means further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

49. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon

a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

50. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

51. (Original) A demodulator according to claim 44 further comprising means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits).

52. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

53. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a bi-orthogonal code.

54. (Original) A demodulator according to claim 44 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

55. (Currently Amended) A method for baseband processor for spread spectrum radio communication, the method comprising the steps of:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to a predetermined orthogonal code,

wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~encoded~~ information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state; and

spread spectrum PSK demodulating received information by decoding the received information according to the predetermined orthogonal code.

56. (Original) A method according to claim 55 further comprising the step of AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

57. (Original) A method according to claim 55 further comprising the steps of modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

58. (Original) A method according to claim 57 further comprising the steps of:

modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

59. (Original) A method according to claim 58 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

60. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a

Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

61. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a bi-orthogonal code.

62. (Currently Amended) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit coupled thereto, said baseband processor comprising a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit, at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to said radio circuit, said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component relative to an unmodified Walsh code for reducing an average DC signal component of the ~~decoded~~ information decoded by the modified Walsh code relative to that information being decoded by the Walsh code in its unmodified state, and a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

63. (Original) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator is configured to operate in one of the first and second formats.

64. (Previously Presented) A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format

defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

65. (Previously Presented) A spread spectrum radio transceiver according to claim 64 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

66. (Original) A spread spectrum radio transceiver according to claim 64 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

67. (Original) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

68. (Original) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

69. (Original) A spread spectrum radio transceiver according to claim 62 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and

magnitude (three bits) to said at least one modified Walsh code function encoder.

70. (Original) A spread spectrum radio transceiver according to claim 62 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

71. (Previously Presented) A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel coupled correlators coupled to said modified Walsh function generator.

72. (Previously Presented) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

73. (Original) A spread spectrum radio transceiver according to claim 62 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

74. (Original) A spread spectrum radio transceiver according to claim 62 wherein said demodulator is configured to generate a clear channel assessment signal.

75. (Previously Presented) A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator coupled to said baseband processor; and

an up/down frequency converter coupled to said quadrature intermediate frequency modulator/demodulator.

76. (Previously Presented) A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:

a low noise amplifier having an output coupled to an input of said up/down converter; and

a radio frequency power amplifier having an input coupled to an output of said up/down converter.

77. (Original) A spread spectrum radio transceiver according to claim 76 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

78. (Currently Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~decoded~~ information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one orthogonal code function encoder for encoding information according to the orthogonal code.

79. (Original) A baseband processor according to claim 78 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator is configured to operate in one of the first and second formats.

80. (Previously Presented) A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

81. (Previously Presented) A baseband processor according to claim 80 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

82. (Original) A baseband processor according to claim 80 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

83. (Original) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

84. (Original) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

85. (Previously Presented) A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder.

86. (Previously Presented) A baseband processor according to claim 78 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

87. (Previously Presented) A baseband processor according to claim 78 wherein the orthogonal code is a bi-orthogonal code.

88. (Previously Presented) A baseband processor according to claim 78 wherein said at least one orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

89. (Previously Presented) A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to generate a preamble; and wherein said demodulator comprises preamble

demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

90. (Original) A baseband processor according to claim 78 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

91. (Previously Presented) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

wherein said modulator is configured to operate in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and

wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising at least one correlator for decoding received information, wherein said demodulator is configured to operate in one of the first and second formats, wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header, a first carrier tracking loop for the third format, and a second carrier tracking loop for the first and second formats.

92. (Previously Presented) A baseband processor according to claim 91 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

93. (Original) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

94. (Original) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

95. (Previously Presented) A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is further configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

96. (Original) A baseband processor according to claim 91 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

97. (Currently Amended) A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one orthogonal code function encoder for encoding information according to an orthogonal code, wherein the orthogonal code is modified

to have a reduced DC component for reducing an average DC signal component of the ~~encoded~~ information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state.

98. (Original) A modulator according to claim 97 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

99. (Previously Presented) A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats.

100. (Previously Presented) A modulator according to claim 99 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

101. (Previously Presented) A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder, and wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

102. (Previously Presented) A modulator according to claim 97 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

103. (Previously Presented) A modulator according to claim 97 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

104. (Previously Presented) A modulator according to claim 97 wherein the orthogonal code is a bi-orthogonal code.

105. (Currently Amended) A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information by spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~decoded~~ information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state.

106. (Original) A demodulator according to claim 105 wherein said demodulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

107. (Previously Presented) A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

108. (Previously Presented) A demodulator according to claim 107 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

109. (Original) A demodulator according to claim 107 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

110. (Original) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

111. (Original) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

112. (Original) A demodulator according to claim 105 further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits).

113. (Previously Presented) A demodulator according to claim 105 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

114. (Previously Presented) A demodulator according to claim 105 wherein the orthogonal code is a bi-orthogonal code.

115. (Previously Presented) A demodulator according to claim 105 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

116. (Currently Amended) A method for spread spectrum radio communication, the method comprising:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the ~~encoded~~ information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state; and

spread spectrum PSK demodulating received information by decoding the received information according to the orthogonal code.

117. (Original) A method according to claim 116 further comprising AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

118. (Original) A method according to claim 116 further comprising modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

119. (Previously Presented) A method according to claim 118 further comprising:

modulating data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

120. (Previously Presented) A method according to claim 119 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

121. (Previously Presented) A method according to claim 116 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

122. (Previously Presented) A method according to claim 116 wherein the orthogonal code is a bi-orthogonal code.

123. (Previously Presented) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence generated at a predetermined chip rate;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences generated at the same chip rate as said spreading sequence and chosen from a set that is substantially orthogonal with low DC components; and

applying the spread-spectrum encoded symbols of said header field and selected chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

124. (Previously Presented) The method of claim 123 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-

bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

125. (Previously Presented) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences chosen from a set that is substantially orthogonal with low DC components, each of said chip sequences being differentially phase encoded;

applying a reference phase based on encoding of the last of said first data symbols to the differential encoding of the first selected chip sequence; and

inputting said encoded symbols of said header field and said differentially encoded chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

126. (Previously Presented) The method of claim 125 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

127. (Previously Presented) A method of generating an rf signal in a transmitter having a phase shift modulator with I and Q inputs comprising the steps of:

supplying a stream of binary information containing header data and payload data, said header data specifying at least a first payload data rate or a second payload data rate;

encoding said payload data when said header data specifies said first payload data rate by grouping said payload data into N-bit symbols, where N is greater than 1, and applying each N-bit symbol to select one of 2^N possible chip sequences and chosen from a set that is substantially orthogonal with low DC components;

encoding said payload data when said header data specifies said second payload data rate by grouping said payload data into 2N-bit symbols and applying each 2N-bit symbol to select one of 2^{2N} possible chip sequences; and

applying each selected chip sequence to the I and Q inputs of said phase shift modulator.

128. (Previously Presented) The method of claim 127 wherein the chip sequences selectable by said 2N-bit symbols include the chip sequences selectable by said N-bit symbols plus 2^{2N}-2^N additional chip sequences.

129. (Previously Presented) The method of claim 127 wherein the chip sequences selected by said N-bit symbols and said 2N-bit symbols are generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit or 2N-bit symbol and differentially phase encoding the selected initial chip sequence in accordance with a second data segment of the same N-bit or 2N-bit symbol.

130. (Previously Presented) The method of claim 127 wherein each of the 2^{2N} chip sequences selectable by said 2N-bit symbols comprises an I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively.

131. (Previously Presented) The method of claim 129 wherein N=4 and wherein each chip sequence selected by a 2N-bit symbol comprises an initial I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively, said initial I/Q chip sequence being selected by 6 bits of a 2N-bit symbol and being differentially phase encoded in accordance with the other 2 bits of the same 2N-bit symbol.

132. (Previously Presented) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences, wherein each chip sequence is M chips in length and is a composite of an M-bit basic sequence and an M-bit modification sequence and chosen from a set that is substantially orthogonal with low DC components;

rotating the phase of the selected chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said chip sequence; and

transmitting each phase-rotated, selected chip sequence at said predetermined chip rate.

133. (Previously Presented) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences chosen from a set that is substantially orthogonal with low DC components, wherein each chip sequence is M chips in length;

combining the selected basic chip sequence with a fixed, M-chip modification sequence to produce a selected M-chip composite chip sequence;

rotating the phase of the selected M-chip composite chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said basic chip sequence; and

transmitting each phase rotated, selected composite chip sequence at said predetermined chip rate.